REMARKS

Claims 1-21 are pending in the present application. Claims 9-13 have been allowed, and claims 2, 4-7 and 15-20 have been objected to for containing allowable subject matter but depending on a rejected base claim. Claims 1, 3, 8 and 14 have been rejected. Claims 1, 3 and 15 have been amended, and claim 21 is new. Reconsideration in view of the following arguments is kindly requested.

Allowable Subject Matter

Initially, Applicants thank the Examiner for indicating that claims 9-13 have been allowed, and that claims 2, 4-7 and 15-20 are objected to for containing allowable subject matter and would be allowable if rewritten into independent form, including all of the features recited in their parenting claims. Further, Applicants note that the Examiner has indicated that claim 3 would also be allowable if amended to overcome a minor claim language informality.

Claim Objections

The Examiner has objected to claim 15 for containing minor claim language informalities. In accordance with the Examiner's suggestions, Applicants have amended claim 15 to clarify the claim language and in an effort to overcome this objection. Applicants submit that the amendment to claim 15 is for clarification purposes only and is not related to the patentability of claim 15. Accordingly, Applicants submit that this objection be withdrawn.

Claim Rejections – 35 U.S.C. § 112

The Examiner has rejected claim 3 under 35 U.S.C. § 112, second paragraph, for being indefinite. In accordance with the Examiner's suggestions, Applicants have amended claim 3 to clarify the subject matter which the Examiner has regarded as indefinite. Applicants submit that the amendment to claim 3 is for clarification purposes only and is not related to the patentability of claim 3. Accordingly, Applicants submit that this rejection be withdrawn.

Claim Rejections – 35 U.S.C. § 103

The Examiner has rejected claims 1, 8 and 14 under 35 U.S.C. § 103(a) over Takada et al., USP 5,955,902 in view of Ho et al., USP 6,426,660. This rejection is respectfully traversed. Applicants submit that references Takada and Ho are not combinable, and the Examiner has not provided any evidence of a suggestion or motivation for combining Takada and Ho. Further, Applicants submit that the reasoning behind the Examiner's motivation for combining Takada and Ho uses impermissible hindsight reconstruction to reject the claims, which is not acceptable.

The Examiner alleges,

> "It would have been obvious...that the XOR gate (32) of Ho could be used to replace the multiplying circuit (38) of Takada (wherein the XOR gate 32 would receive the first clock signal (Fref/F1) and the delayed clock signal Fdel) for the advantage of being able to generate a second clock signal (OUTPUT CLOCK) having a 50% duty cycle".

The Examiner has failed to provide any evidence of motivation why the XOR gate in Ho would be used in the logic circuit of Takada, or more specifically evidence as to why one of ordinary skill in the art would be motivated to remove the RS flip-flop from Takada and replace it with the XOR gate in Ho, which is connected to a reduced duty-cycle clock signal and a further reduced rate clock signal derived from the reduced duty-cycle clock signal (See Fig. 1 of Takada and Fig. 3 of Ho).

This shortcoming of Takada which must be supplemented by some other teaching wherein one of ordinary skill in the art must be motivated to provide the supplemental teaching by some motivation, teaching or suggestion of the desirability to make the combination as indicated in In re Dembiczak, 50 USPQ2d 1646 (Fed. Cir. 1999) and In re Kozab, 55 USPQ 1313 (Fed. Cir. 2000).

Further, the Examiner is using impermissible hindsight reconstruction to reject the features recited in claim 1. For instance, the Examiner's statement noted above, concludes that the XOR gate disclosed in Ho could be used in Takada, thus there is sufficient evidence that Takada and Ho

are combinable. Applicants disagree with the Examiner's reasoning, and submit that the mere possibility that one element in one reference could be used in another is not sufficient evidence of a suggestion or motivation to combine the two references.

Applicants submit the Examiner has used the present application as a blueprint, selected a prior art frequency multiplier structure (Takada) as the main structural device, and then searched other prior art for the missing XOR gate, without identifying or discussing any specific evidence of motivation to combine, other than providing conclusory statements regarding the knowledge in the art, motivation and obviousness. The Federal Circuit has noted that the PTO and the courts "cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention," In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1780, 1783 (Fed. Cir. 1988), and that the best defense against hindsight-based obviousness analysis is the rigorous application of the requirement for a showing of a teaching or motivation to combine the prior art references. Applicants submit that the Examiner has failed to provide evidence of motivation for combining the teachings of Takada and Ho.

Accordingly, the Examiner has not adequately supported the selection and combination of Takada and Ho to render claim 1 as obvious.

Assuming *arguendo* the teachings of Takada and Ho were combinable, which Applicants do not admit to, then the combination of references fail to teach all of the claim limitations recited in claim 1. In order to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a) all of the claim limitations of the rejected claim must be contained in the references.

Applicants agree with the Examiner that Takada fails to teach or disclose an XOR gate that receives a first clock signal and a delayed clock signal, and performs an XOR operation on the first clock signal and the delayed clock signal, and outputs a second clock signal, as recited in claim 1. However, Applicants disagree that Ho teaches these shortcomings of Takada.

Takada discloses a delay circuit with an input signal Fref that is inputted into a VCD 31. The output of VCD 31 includes signals F1-F2N and Fdel. None of the signals F1-F2N received by logic circuit 38 include the original input signal Fref. Ho discloses a duty-cycle correction circuit 10, which divides an input clock signal by 2, at a frequency divider 12, and inputs the half duty-cycle signal into a clock doubler circuit 14, which includes an XOR gate 32. The half duty-cycle signal, and a further delayed version of the half duty-cycle signal output from the current control delay block 30, are provided to the XOR gate 32. See Figs. 1 and 3, and column 3, lines 17-26 of Ho.

Applicants submit that Ho does not disclose the features recited in claim 1, as the input signals of the XOR gate are both delayed signals derived from the input clock signal originating from the clock source 16. See Figs. 1 and 3 of Ho. The inputs to the XOR gate disclosed in Ho do not teach an XOR gate that receives a first clock signal and a delayed clock signal, and performs an XOR operation on the first clock signal and the delayed clock signal, and outputs a second clock signal, as recited in claim 1.

Accordingly, for at least this additional reason, claim 1 and those claims dependent thereon are allowable over the prior art. Withdrawal of this rejection is kindly requested.

Regarding claim 14, Applicants submit for similar reasons to those stated above with regard to claim 1, that claim 14 and those claims dependent thereon are also allowable over the prior art. Withdrawal of this rejection is also kindly requested.

Newly added claim 21 is directed to a method which includes, comparing a first voltage corresponding to a first clock signal, to a second voltage corresponding to a delayed clock signal, and outputting a signal to increase the level of a digital control signal if the difference between the first and second voltages is greater than a threshold value, and outputting a different signal to decrease the digital control signal level if the difference between the first and second voltages is less

than the threshold value. Applicants submit that none of the references noted above disclose these features, or render them as obvious.

Accordingly, Applicants submit that for at least the reasons stated above, all currently pending claims 1-21 are in condition for allowance. Withdrawal of any outstanding rejections and an allowance of these claims is kindly requested.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-21 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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By _____
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